UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,554	01/23/2004	Hirokazu Honda	NEC 26485	7561

27667 7590 09/04/2009

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE, SUITE 140
TUCSON, AZ 85718

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
09/04/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

admin@hayes-soloway.com
smckniff@hayes-soloway.com
nsoloway@hayes-soloway.com

Office Action Summary	Application No.	Applicant(s)	
	10/763,554	HONDA, HIROKAZU	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-20* is/are pending in the application.

4a) Of the above claim(s) *10-15,18 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,16,17 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/23/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/763554 Attorney's Docket #: NEC 26485
Filing Date: 1/23/2004; priority to 2/3/2003 and 12/10/2003

Applicant: Honda

Examiner: Alexander Williams

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/23/09 has been entered.

Applicant's Amendment filed 6/23/09 to the election of the species I, figures 1a, 1b, 8a-8h and 12a (claims 1-9, 16-18 and 19), filed 9/26/05, has been acknowledged.

This application contains claims 10-15, 18 and 19 drawn to an invention non-elected without traverse.

Claims 2 and 3 have been cancelled.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-9, 16, 17 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Soga et al. (U.S. Patent # 4,970,575) in view of Baba Mikio (Japan Patent Publication # 2001-244362 A).

1. Soga et al. (figures 1 to 8) specifically figures 1 and 6C show a semiconductor device comprising: a semiconductor chip **1** mounted on a mounting substrate **9**; a first resin **(portion of 11 under the chip)** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **17** surrounding the semiconductor chip; and a second resin **(outer portion of 11)** partially filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; a second resin filling a space between the semiconductor chip and the stiffener in contact with the first resin, wherein the first and second resin comprises an epoxy resin main component and an inorganic filler component and wherein the epoxy resin main component is the same in the first resin and the second resin and the inorganic filler component of the first resin is different in content amount than the inorganic filler component of the second resin.

(10) In order to achieve the above-stated object, in the present invention, either an epoxy resin or a resin having a lower coefficient of thermal expansion than the epoxy resin is used, an inorganic material having a still smaller thermal expansion coefficient than said resin is mixed in the resin, and a vacant space around solder bumps is filled up with the mixture thus prepared.

(11) According to the present invention, the thermal expansion coefficient of the resin approximates that of the solder bumps, and thermal stress caused by the difference in the coefficient of thermal expansion between a chip and a substrate is received by the entire resin having a large expansion rigidity.

Therefore, destruction due to local strains of solder bumps located in the outermost peripheries, which is seen in the prior-art device, is eliminated, and the deformation of the solder due to the deformation of the resin causes no substantial burden, because of the absence of constraints.

(3) For this purpose, an inorganic material having a small thermal expansion coefficient, such as silica powder, is mixed in an epoxy resin or a polyimide resin having a smaller thermal expansion coefficient than the epoxy resin, so as to lower the degree of expansion. When silica powder of 50% in volume is mixed in for instance, the thermal expansion coefficient .alpha. lowers to about 25.times.10.sup.-6 /.degree.C. this value is equal to the value of the thermal expansion coefficient of the solder itself and therefore the deformation of the solder is in accord with that of the resin having a large expansion rigidity. Thus, the concentration of stress of solder bumps located in the outermost peripheries is expected to be eliminated. With an increase in the mixing rate of the silica powder, however, the viscosity of the resin increases, and when the fluidity thereof lowers consequently, it becomes difficult for the resin to flow into the vacant space formed around solder bumps in a coating process. This causes such problems that vacant portions are left, that the adhesiveness to the substrate is reduced, that the operability of coating is decreased, etc. These problems are sometimes accompanied by contradictory results that resistance to thermal fatigue and resistance to humidity are reduced. When vacancies as large as bubbles are left in the vicinity of the solder bumps, for instance, the concentration of stress is intensified in the vicinity of the vacancies. A thermal cycle test revealed that the thermal fatigue service life of a sample having these vacancies was significantly shorter than that of a sample completely filled with the resin. In a humidity resistance test performed by means of a high-temperature protracted test, in which lifetimes were compared with means of a continuity check, it was also revealed that the humidity resistance of the former sample was apparently lower than the latter.

(13) Next, a description will be made on the shape of a resin coat. Even when the expansion-reducing material such as silica powder is mixed in, as described above, the thermal expansion coefficient .alpha. of the epoxy resin is still a larger value than those of the substrate and the Si chip, and the Si chip, solder bumps, the substrate, or the connecting parts of these

members, are damaged by a stress caused by the difference between the members. Experiments revealed that the connecting part of the solder bumps with the Si chip was the weakest of all to a repeated stress.

Soga et al. fail to explicitly show a stiffener surrounding the semiconductor chip, the stiffener being adhered to the mounting substrate with a first adhesive.

Baba Mikio is cited for showing a semiconductor device. Specifically, Baba Mikio (figures 1 to 4) particularly figure 1 show a semiconductor device comprising: a semiconductor chip **2** mounted on a mounting substrate **1**; a first resin **6** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **5** surrounding the semiconductor chip, the stiffener being adhered to the mounting substrate with a first adhesive **4**; and a second resin **7** partially filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin for the purpose of enhancing a flip chip device in heat dissipating properties and an inter-pad connection between the flip device and a ceramic package in reliability.

4. The semiconductor device as claimed in claim 1, the combination with Sogo et al. show wherein the first resin includes an underfill part filling the gap between the semiconductor chip and the mounting substrate, and a fillet part extended from a region of the semiconductor chip.

5. The semiconductor device as claimed in clam 1, the combination with Mikio show wherein the first adhesive is larger in a thermal expansion coefficient than the second resin.

6. The semiconductor device as claimed in claim 4, the combination with Mikio show wherein the second resin **22** is in contact with inner walls of the stiffener **1**, the fillet part **21**, the mounting substrate **1** and each of side faces of the semiconductor chip **2**.

7. Soga et al. (figures 1 to 8) specifically figures 1, 6C and 7A show a semiconductor device comprising: a semiconductor chip **1** mounted on a mounting substrate **9**; a first resin **(portion of 11 under 1)** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **17** surrounding the semiconductor chip, the stiffener being made of a different material from the second resin; a second resin **(portion of 11 around 1)** filling a space on the outer side of the semiconductor chip and in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; and a lid **22** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive.

Soga et al. fail to explicitly show a stiffener surrounding the semiconductor chip, a second resin filling a space between the semiconductor chip and the stiffener in contact with the first resin.

Baba Mikio is cited for showing a semiconductor device. Specifically, Baba Mikio (figures 1 to 4) specifically figure 1 show a semiconductor device comprising: a semiconductor chip **2** mounted on a mounting substrate **1**; a first resin **6** filling a gap between the semiconductor chip and the mounting substrate; a stiffener **5** surrounding the semiconductor chip, the stiffener being made of a different material from the second resin; a

second resin **4** filling a space between the semiconductor chip and the stiffener in contact with the first resin, the first resin being different in a thermal expansion coefficient from the second resin; and a lid **9** for covering the stiffener and the semiconductor chip, wherein the lid is bonded to the stiffener and a backside of the semiconductor chip with an adhesive for the purpose of reducing the problem of reducing drawing the moisture to expand under the environment of the high temperature and the high humidity, allowing the resistance to increase.

8. The semiconductor device as claimed in claim 7, the combination with Mikio show wherein the second resin **22** is in contact with an inner wall of the lid.

9. The semiconductor device as claimed in claim 1, the combination with Mikio show wherein an elastic modulus of the second resin **22** is larger than an elastic modulus of the first resin **21**.

16. The semiconductor device as claimed in claim 1, the combination with Mikio show wherein the stiffener **(outer portion of 5)** is made of a material selected from the group consisting of Cu, SUS, Al, alumina, silicon, aluminum nitride, and resin.

17. The semiconductor device as claimed in claim 1, the combination with Mikio show wherein each of the first resin **21** and the second resin **22** essentially contains a resin selected from a group consisting of **epoxy**, polyolefin, silicon, cyanate ester, polyimide, polynorbornene resins.

20. The semiconductor device as claimed in claim 1, the combination with either reference showing wherein the semiconductor chip is mounted on the mounting substrate through flip chip bonding.

Therefore, it would have been obvious to one of ordinary skill in the art to use Mikio's stiffener with the second resin to modify Soga et al.'s second resin for the purpose of enhancing a flip chip device in heat dissipating properties and an inter-pad connection between the flip device and a ceramic package in reliability.

Response

Applicant's arguments filed 6/23/09 have been fully considered, but are not found to be persuasive view of the new grounds of rejections detailed above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AOW
8/31/09

/Alexander O Williams/
Primary Examiner, Art Unit 2826